REMARKS

By this submission accompanying with a request for continued examination, claims 6, 11 and 14 have been amended. Accordingly, claims 3, 6, 9, and 11-15 are pending in this application and are respectfully submitted for a timely examination.

Rejection of Claims 11-13 under 35 U.S.C. § 103(a)

Claims 11-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,349,366, "Yamazaki") in view of Dawson et al. (U.S. Patent No. 6,229,506, "Dawson"). The Applicants respectfully traverse the rejection.

Claim 11 as amended, recites a display device comprising, among other features, a ferroelectric capacitor connected between a gate of a MOS transistor and a control line wherein the control data is written to the ferroelectric capacitor by using a control line and a ground or a write line, and wherein said ferroelectric capacitor maintains a floating state while the control data is written thereto.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Yamazaki merely disclose an electro-optical display device operating in an active matrix mode. The device of Yamazaki includes pixels each provided with a first element for selecting the pixel, a second element for supplying electric current to the pixel in accordance with the information transferred from the first element, and a memory element which stores the signal having output from the first element. Yamazaki also provides a method of displaying images using an electro-optical display device operating in an active matrix mode, the method having rewriting only the specified pixels, or comprising rewriting only the specified lines during one frame, or comprising

taking the period of scanning (addressing) the image plane longer than the period of alternating the polarity of the electric current applied to the pixels.

Dawson discloses a LED pixel structure that reduces current non-uniformities and threshold voltage variations in a "drive transistor" of the pixel structure. The LED pixel structure of Dawson incorporates a current source for loading data into the pixel via a data line. Alternatively, an auto zero voltage is determined for the drive transistor prior to the loading of data.

The Applicants submit that Yamazaki in view of Dawson fail to disclose or suggest each and every element recited in claim 11 of the present application. For instance, it is submitted that the capacitor of Dawson is neither comparable nor analogous to the capacitor connected between said gate and a ground or a write line, as recited in the present invention. Specifically, Dawson purports to apply voltage exceeding a particular value to the gate of the drive transistor 460 and repeats charge to the capacitor C_S and display in each frame.

In addition, the capacitor C_S of Dawson is not connected in the floating state. As disclosed in one example of the present invention on page 18, lines 2-18, one electrode of the ferroelectric capacitor must be insulated not by the source/drain or wiring of a transistor but by gate insulation film or capacitor. In contrast, Dawson merely shows one electrode of C_S is connected to the OLED via the source and drain of the transistor 465, and when actually charged, a small amount of current trickles into the OLED (see, column 5, lines 55-58 of Dawson). Consequently, even if assuming the electrode of Dawson is connected to the gate of the transistor 460 (not admitted), there is a patch through which electric charge leaks. Furthermore, even if assuming that the capacitor

C_S is replaced with a ferroelectric capacitor (not admitted), the Applicants submit that it is not possible to hold the display data which is not changed, as is the case of the present invention.

In addition, it is submitted that the path to charge the capacitor C_S of Dawson begins with VSWP and ends with OLED via the transistor 465 as described above, which is not the path which passes the capacitor C_c . As such, the Applicants submit that there is no capacitor of Dawson which is inserted in the data writing route and holds data with care to prevent data from disappearing while writing data.

Hence, it is submitted that the cited prior art fails to disclose or suggest at least "the control data is written to said ferroelectric capacitor by using said control line and said ground or said write line, and wherein said ferroelectric capacitor maintains a floating state while the control data is written thereto."

In essence, the Applicants submit that Dawson connects capacitor C_S between the gate and the source of a driver transistor for the mere purpose of applying overdrive voltage to the gate of the drive transistor 460 and stabilizing the current to OLED. And one electrode of the capacitor C_S is connected to VSWP and the other electrode is connected to OLED via the source of the transistor 465. Consequently, the Applicants further submit that the capacitor C_S of Dawson has both electrodes connected to sources of transistors 460 and 465, and therefore is NOT brought into the floating state. Furthermore, the capacitor C_S fails to NOT rewrite the display data when the display data is not required to be rewritten in a different frame.

Therefore, Applicants submit that Yamazaki in view of Dawson fails to disclose each and every element recited in claim 11 of the present application, and is therefore allowable.

As claims 12-13 depend from claim 11, the Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, the Applicants respectfully request withdrawal of the rejection.

Rejection of Claims 3, 6, 9 and 15 under 35 U.S.C. § 103(a)

Claims 3, 6 and 9 (Office Action mistakenly included claim 15, which depends on claim 14) were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Dawson and further in view of Black et al. (U.S. Patent No. 6,069,381, "Black"). The Applicants respectfully traverse this rejection.

Independent claim 6 recites in part:

> ...a capacitor connected between said second metal layer and a ground or a write line,
>
> wherein the control data is written to said MFMIS structure transistor by using said control line and said ground or said write line, and
>
> wherein the MFMIS structure transistor maintains a floating state while the control data is written thereto.

The Office Action admits that Yamazaki in view of Dawson fails to teach and/or suggest a "transistor that is an MFMIS structure transistor which has a first metal layer, a ferroelectric layer, a second metal layer for gate electrode and an insulator layer provided on a semiconductor layer, a source and drain of said MFMIS structure

transistor." The Office Action refers to Figure 7 of Black as allegedly teaching "an MFMIS structure transistor which as a first metal layer (5), a ferroelectric layer (2), a second metal layer (7) for gate electrode and an insulator layer provided on a semiconductor layer (8), a source and drain (9) of said MFMIS structure transistor (col. 4, lines 46-67, col. 6, lines 1-13). The Applicants respectfully disagree with the Examiner's characterization of the cited prior art, especially Black.

The Applicants submit that Yamazaki in view of Dawson and further in view of Black fail to disclose or suggest each and every element recited in claim 6 of the present application. For at least the reason provided above, it is submitted that Yamazaki in view of Dawson fails to disclose or suggest at least the features of "a MFMIS structure ... wherein the control data is written to the MFMIS structure transistor by using said control line and said ground or said write line, and wherein the MFMIS structure transistor maintains a floating state while the control data is written thereto." Black fails to cure the deficiencies of Yamazaki in view of Dawson.

Therefore, the Applicants submit that Yamazaki in view of Dawson further in view of Black fail to disclose each and every element recited in claim 6 of the present application, and is therefore allowable.

As claims 3 and 9 depend from claim 6, the Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, the Applicants respectfully request withdrawal of the rejection.

Rejection of Claim 14 under 35 U.S.C. § 103(a)

Claim 14 was rejected under 3535 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Black and further in view of Hidaka et al. (U.S. Patent No. 6,521,927). The Applicants respectfully traverse the rejection.

Claim 14 recites a display device comprising, among other features, a nonvolatile data holding section integrated with said control element or connected to said control element and capable of holding control data of said control element in a floating state; wherein said nonvolatile data holding section is constituted by an element utilizing a magnetoresistance effect or a single electron memory having electrons stored in quatum dot over a barrier region.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

In making the rejection, the Examiner took the position that "Yamazaki and Black teaches all the limitations except the nonvolatile data holding section is constituted by an element utilizing a single electron memory." The Applicants respectfully disagree.

It is submitted that Yamazaki in view of Black fails to disclose or suggest at least "a nonvolatile data holding section integrated with said control element or connected to said control element and capable of holding control data of said control element in a floating state." In fact, the Examiner failed to even address these features in the Office Action. Furthermore, the Applicants submit that Hidaka fails to cure this deficiency of the cited prior art.

Therefore, the Applicants submit that Yamazaki in view of Black further in view of Hidaka fail to disclose each and every element recited in claim 14 of the present application, and is therefore allowable.

Accordingly, the Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, the Applicants respectfully request the allowance of claims 3, 6, 9, and 11-15 and the prompt issuance of a Notice of Allowance.

Should the Examiner believe anything further is desirable in order to place the application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing Attorney Docket No. 107400-00021.

Respectfully submitted,

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